Digital Design Principles

Octal Decoder

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Objective:

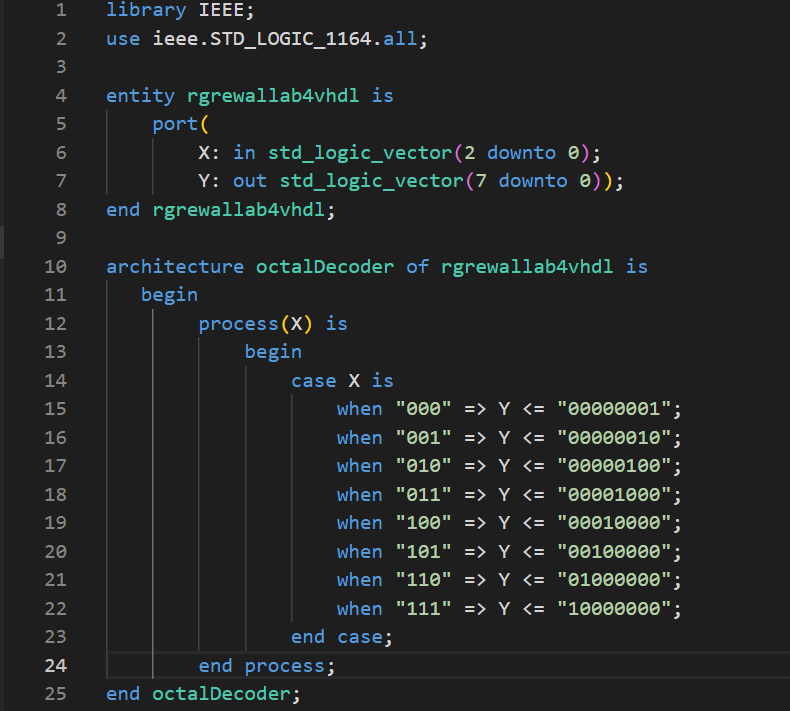
- Explore the use of concurrent constructs to model combinational logic circuits.  
- Model an octal decoder circuit using conditional assignment.

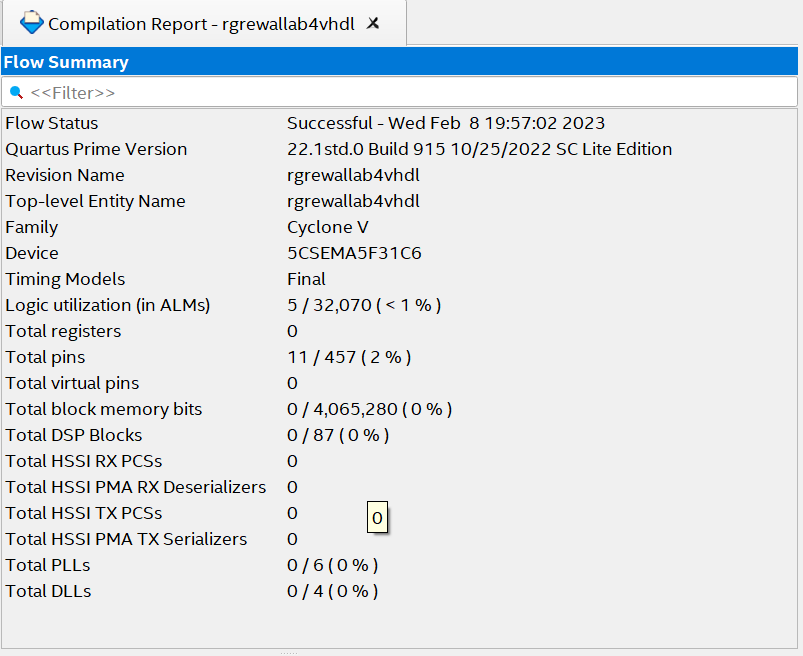
Truth Table:

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| X2 | X1 | X0 | Y7 | Y6 | Y5 | Y4 | Y3 | Y2 | Y1 | Y0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

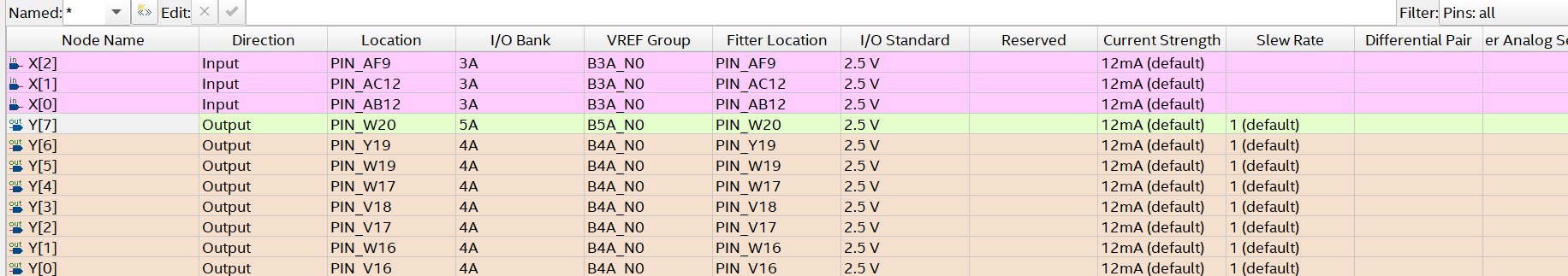
VHDL Introduction:

To make the program in VHDL we will need to initialize the library and entity. Within the entity we will state the 3 input switches and the 8 output LEDs. Within the architecture of the program we will use case and when statement. Where for each different state the three inputs are the according led will be set to light up. The above truth table is the be followed to know which led is to be set accordingly.

VHDL program screenshot:

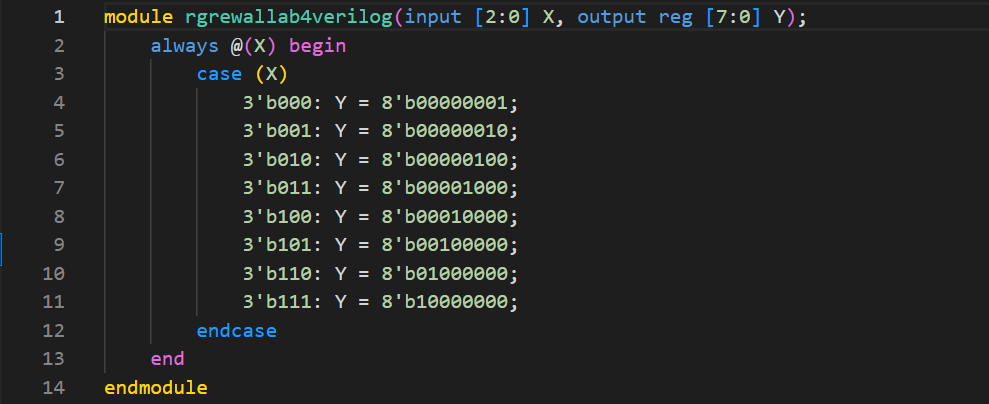
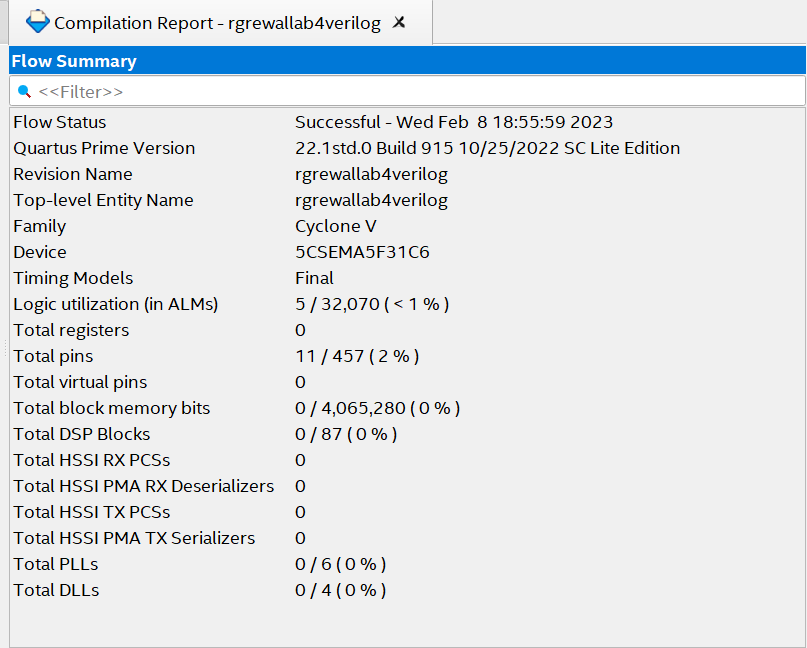
VHDL compilation report:

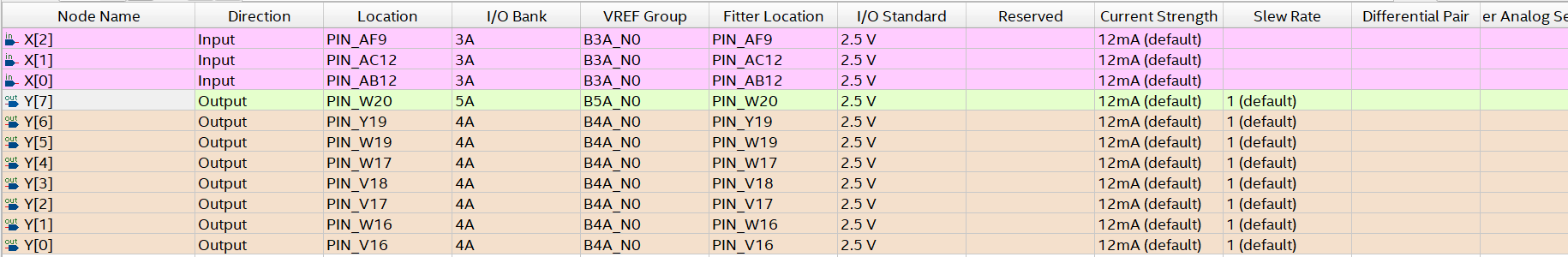
Pin Planner screenshot:



Verilog introduction:

For the program in Verilog we will need to initialize the module with the parameters having the three inputs and eight outputs. Within the module block we use case where the output will assign the value according to the state of the input which matches to the truth table.

Verilog program screenshot:Verilog compilation report:

Verilog pin planner screenshot:

Conclusion:

Thus we can conclude that by both the programming languages we will use case statement and the one led which corresponds to the input will light up. The above truth table will be followed thus creating our octal decorder.